UC Riverside
UC Riverside Previously Published Works

Title

Interposer-Based ESD Protection: A Potential Solution for μ-Packaging Reliability of 3D Chips

Permalink

https://escholarship.org/uc/item/4k04s9g7

Journal

Micromachines, 16(4)

ISSN

2072-666X

Authors

Li, Xunyu
Pan, Zijin
Hao, Weiquan
et al.

Publication Date

2025

DOI

10.3390/mi16040488

Peer reviewed

eScholarship.org Powered by the California Digital Library
University of California

micromachines

MDPI

Perspective

Interposer-Based ESD Protection: A Potential Solution for μ-Packaging Reliability of 3D Chips

Xunyu Li, Zijin Pan, Weiquan Hao, Runyu Miao, Zijian Yue and Albert Wang *

Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521, USA
* Correspondence: aw@ece.ucr.edu

Abstract: The ending of Moore's Law calls for innovations in integrated circuit (IC) technologies and chip designs. Heterogeneous integration (HI) emerges as a pathway towards smart future chips for more Moore time and for beyond-Moore time, featuring systems-on-integrated-chiplets (SoICs) and advanced micro-packaging (μ-packaging). Reliability, particularly with regard to electrostatic charge (ESD) failure, is a major challenge for 3D SoIC chips in μ-packaging, which is an emerging design-for-reliability challenge for future chips. This perspective article articulates that interposer-based ESD protection will be an important potential solution for 3D SoIC chips in μ-packaging against the devastating ESD failure problem.

Keywords: AI; CDM; chip; ESD protection; heterogeneous integration; IC; interposer; reliability; SoIC; μ-packaging

check for updates

Academic Editors: Liangxing Hu, Youngwoo Kim and Peng Zhao

Received: 26 March 2025
Revised: 17 April 2025
Accepted: 18 April 2025
Published: 21 April 2025

Citation: Li, X.; Pan, Z.; Hao, W.; Miao, R.; Yue, Z.; Wang, A. Interposer-Based ESD Protection: A Potential Solution for μ-Packaging Reliability of 3D Chips. *Micromachines* **2025**, *16*, 488. https://doi.org/10.3390/mi16040488

Copyright: © 2025 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Motivation

Semiconductors and integrated circuits (ICs) have forever changed human life, with microelectronics chips penetrating into every sector of modern society. Since the invention of transistors and ICs [1–4], Si complementary metal-oxide-semiconductor (CMOS) technologies have been relentlessly advancing at a pace driven by Moore's Law [5]. Nevertheless, simple CMOS scaling is rapidly approaching its physical limitation and the ending of Moore's Law urgently calls for disruptive innovations in IC technologies in order to sustain the continuous advances in microelectronics needed to meet the demand for the higher performance of chips. Fortunately, heterogeneous integration (HI) has emerged and opened a pathway towards smart future chips that can deliver not only extreme performance, but also rich functionalities, while ensuring affordability [6]. In a nutshell, HI technologies hetero-integrate different devices made in dissimilar materials using different technologies into a superchip of higher performance and more functionalities, mainly leveraging CMOS IC process platforms. These devices of different functions are broadly called chiplets (generally on the same materials platform) or dielets (typically when using different materials), which can be put together into systems-on-integrated-chiplets (SoICs), as depicted in Figure 1. The IC-scale integration makes SoICs comparable to monolithic systems-on-chip (SoC) in terms of performance, footprint and costs. Critically, reliability and packaging are the two key factors that vitally affect HI/chiplet-based SoIC chips [7].

Advanced packaging plays a key role in realizing HI-enabled SoIC chips where materials and processing innovations are required to address important attributes such as performance (e.g., chiplet-to-chiplet data bandwidth), thermal management (e.g., cooling), integrability, manufacturability, yield and costs, etc. Uniquely, CMOS fabrication technologies can be used to achieve micro-packaging (μ-packaging), realizing fine-pitch critical

dimensions on packaging substrates (or any carrier media) down to the μm to nm level, in order to make SoICs similar to SoCs in terms of both performance and footprint, something which is entirely different from traditional packaging technologies at board level, e.g., for conventional systems-in-packaging (SiP). As such, advanced 3D μ-packaging emerges as a vital technology in modern chip design and fabrication today, with, for example, the highly successful chip-on-wafer-on-substrate CoWoS packaging technology [8,9]. Key technical features enabling μ-packaging include 2D/2.xD/3D packaging, various packaging substrates (e.g., Si, glass, organic), ball bonding, through vias (e.g., through-silicon via, aka, TSV), passive and active interposers, embedded bridges (e.g., Si bridge), micro bumps, copper pillars, Cu–Cu bonding, integrated passive devices (IPDs), flip-chip, 3D stacking, ball grid arrays (BGAs), fine-pitch interconnect fabrics, redistribution layers (RDLs), wafer-level packaging (WLP), etc. [6]. Essentially, today's μ-packaging is quite similar to, and requires concurrent engineering with, IC fabrication.

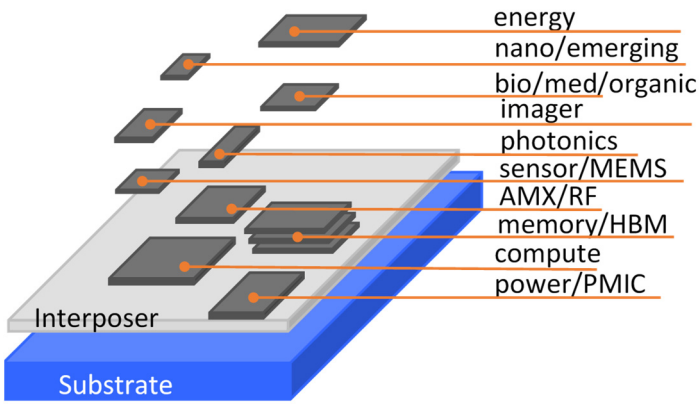

Figure 1. Conceptual illustration of HI-enabled chiplet-based SoIC with rich functionalities and featuring an interposer.

Reliability is a major challenge for making SoIC chips of high performance and at affordable cost because heterogeneous integration makes reliability much more complicated [10,11]. While many reliability problems exist for HI technologies and microsystems, electrostatic discharge (ESD) is particularly challenging for SoIC chips in advanced μ-packaging [12,13]. What makes ESD reliability extremely complicated and ESD protection designs very challenging is the heterogeneity—the core nature of HI technologies. SoIC chips typically have numerous functional domains, such as, logic and compute (e.g., CPU, GPU, AI engine), analog and mixed-signal (AMX), memories (e.g., high-bandwidth memories, aka, HBM), radio-frequency (RF) wireless, power supplies and power management ICs (PMIC), ultra-low power CMOS, high-voltage high-power (HV/HP), energy conversion (e.g., solar), optoelectronics and photonics (e.g., lasers), sensors and actuators, MEMS/NEMS, organic and bio-medical electronics, imagers (e.g., CMOS/CIS), quantum, neuromorphic computing, and various emerging and nano device functions. Similarly, SoICs/μ-packaging involves various different materials (from Si to compound semiconductors, ultra/wide-band gap semiconductors, low-dimensional and nano materials, organic, etc.), complex chip architectures, and complicated physical boundaries. Together, heterogeneous integration and SoIC not only makes ESD protection design more difficult, but also often leads to unexpected new ESD phenomena.

2. Interposer-Based ESD Protection for Chips in μ-Packaging

2.1. ESD Protection and Design Challenges

Electrostatic discharging occurs when two objects of different electric potentials are brought together, either in direct contact or in close proximity. Electrostatic charges will

exchange in between, which produces fast and large current (I) and voltage (V) pulses that can easily damage ICs [14,15]. ESD failure remains a major IC reliability problem to a global microelectronics industry seeking a revenue of ~USD 940 billion by 2030 [16]. On-chip ESD protection is hence required for every IC chip. In principle, an ESD protection structure is placed at a bonding pad on a chip that acts as a controlled switch device, depicted in Figure 2a. The ESD protection switch remains OFF during normal IC operations. When an ESD transient appears at a pad, the ESD switch device will be swiftly turned on to a low-resistance (R_{ON}) conduction path to discharge the incident ESD pulse into ground (GND), hence protecting the IC [14]. Figure 2b illustrates a typical snapback I-V characteristic for an ESD protection structure, showing ESD-critical parameters—including triggering voltage, current and time (V_{t1}, I_{t1}, t_1), holding voltage and current (V_h, I_h,), discharging resistance (R_{ON}), and second breakdown voltage and current (V_{t2}, I_{t2},)—which must be accurately designed in order to comply with the corresponding ESD design window bounded by the supply voltage (V_{DD}), IC breakdown voltage (i.e., safe operation voltage, V_{safe}), total supply current (I_{supply}) and the maximum sustainable current (I_{Fail}), as depicted in Figure 2b [17–19]. It is important to know that ESD protection is a full-chip design task. As depicted in Figure 3, full-chip ESD protection ensures that there always exists a low-R discharging path between any two pads on a chip against any incident ESD pulses [19]. Specifically, since an ESD transient may have positive or negative polarity and an ESD switch device is typically one-directional (i.e., optimized for discharging in one direction), multiple ESD protection structures are generally needed per pad to discharge ESD pulses from a pad positively and negatively with respect to positive supply bus (V_{DD}) and negative supply lines (V_{SS} or GND), commonly marked as PD/ND, PS/NS, and DS/SD ESD stressing modes, respectively. In addition, ESD design overhead always exists and includes ESD-induced parasitic effects, such as parasitic capacitance (C_{ESD}), leakage (I_{leak}), and noises, which seriously affect IC performance. In addition, the large size of ESD devices makes whole-chip layout difficult [20]. ESD design overhead becomes a significant design problem for advanced ICs, which often have large numbers of pads, as shown in Figure 4 [21]. Overall, ESD protection design becomes increasingly more involving and challenging for advanced ICs at advanced technology nodes, particularly for HI/chiplet-based SoIC chips using advanced μ-packaging.

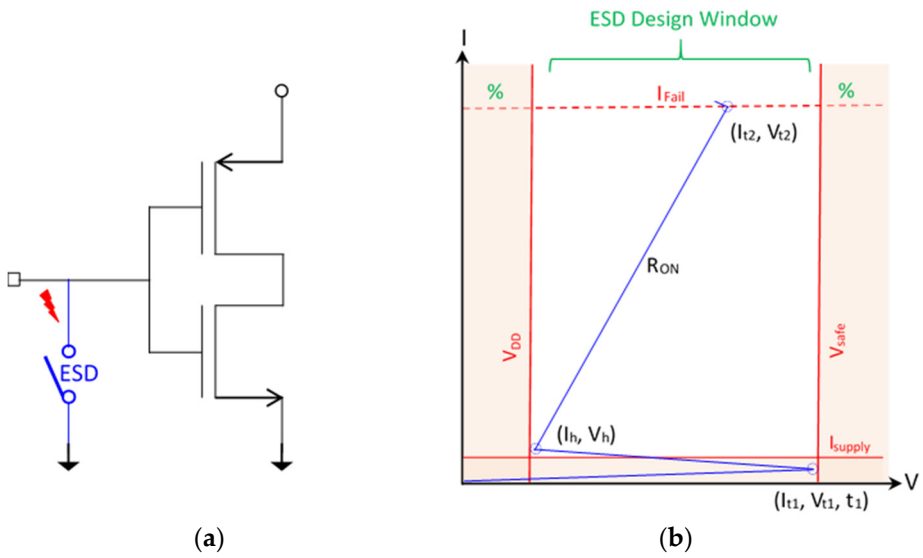

Figure 2. ESD protection concepts: (**a**) an ESD protection device functions as a switch, and (**b**) typical snapback I-V curve of on-chip ESD protection structure featuring ESD-critical parameters that must be designed to comply with an ESD design window.

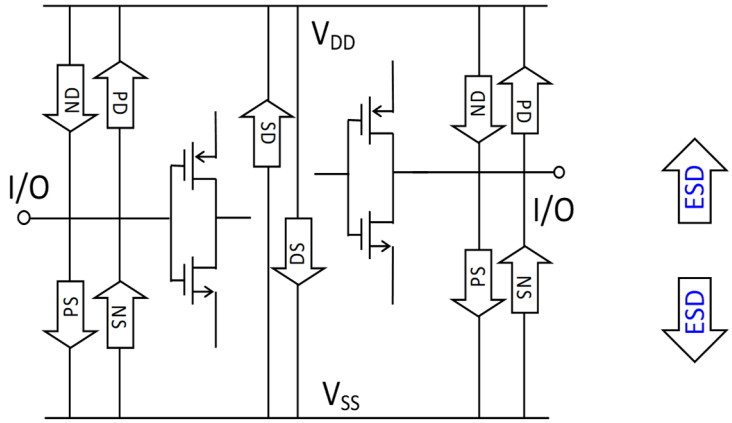

Figure 3. Full-chip ESD protection often requires multiple ESD protection devices per pad to ensure a low-R discharging path between any pairs of bonding pads on a chip. (Arrow boxes representing ESD switch devices in forward low-R conduction mode).

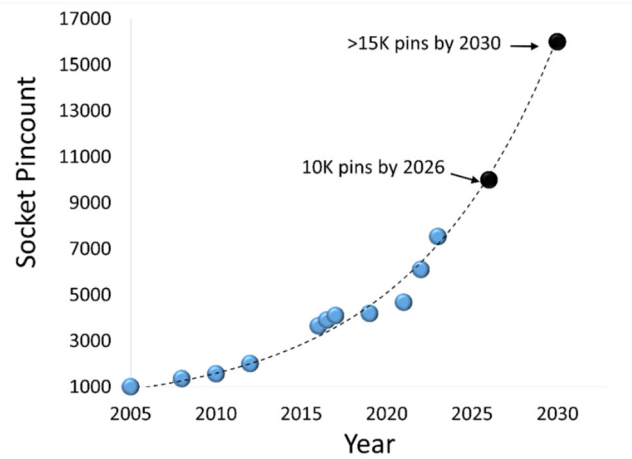

Figure 4. Pad/pin counts for high-performance compute chips increases exponentially over years [21].

2.2. Novel Interposer-Based ESD Protection

As discussed previously, the ESD design overhead effect emerges as a major challenge to large/complex chips because the inevitable ESD-induced parasitic parameters can seriously affect IC performance; while large ESD device-head counts not only consume chip area but also complicate chip layout floor planning. The ESD protection design problem becomes much more complicated for SoIC chips due to domain (functional, materials, technology) diversity and interface/boundary (materials, chiplets) complexity. We envision that interposer-based ESD protection will be an important potential solution for smart future SoIC chips in μ-packaging.

Interposer is a critical technology in 2D/3D ICs and advanced packaging and one that can be used to address the pad/pin pitch mismatch between dies, middle layers and packaging substrate [22]. Typically, a Si interposer serves as an intermediate layer containing complex metal interconnects and through-silicon vias (TSV) to connect chiplets and packaging substrate laterally and vertically, as shown in Figure 1. Interposer technology enables die-level packaging (i.e., IC-scale critical dimensions), supporting heterogeneous integration and terabyte/s high-bandwidth interconnects between dielets. Interposers include Si interposers, organic interposers, glass interposers and embedded interposers (i.e., Si bridges) [23–27]. A passive interposer contains through-vias (e.g., TSV), copper redistributed layer (RDL), Si bridge, and various bonding elements (e.g., micro bumps, copper pillars, Cu–Cu bonding, ball grid arrays, etc.). Recently, active interposers have been

developed that contain high-performance integrated passive devices (IPDs) and various supporting circuitry, e.g., clocks, μ-controllers and high-speed links [28–31]. Figure 5 illustrates a double-sided active interposer for HI/chiplet-based SoIC and μ-packaging with many advanced circuit features.

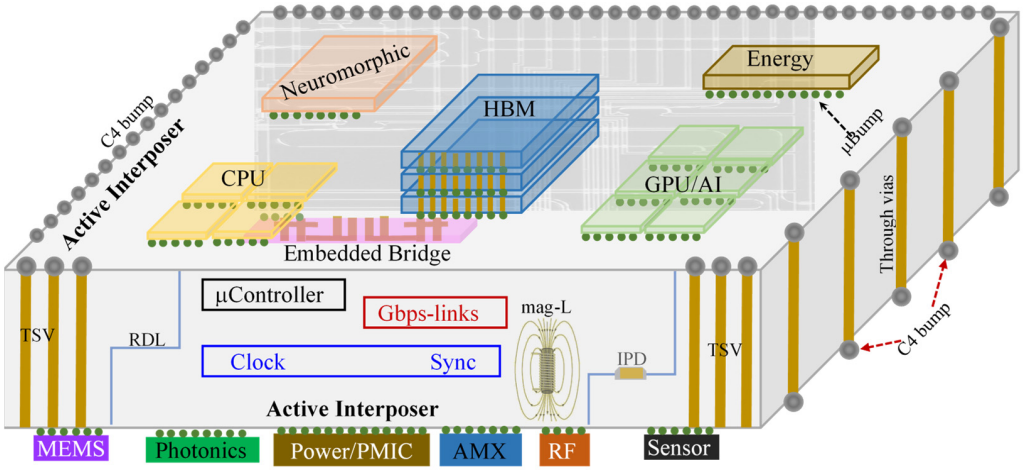

Figure 5. Illustration of a conceptual double-sided active interposer for SoIC packaging (not drawn to scale).

Clearly, interposers in advanced packaging offer room to host ESD protection structures for both SoC and SoIC chips. In principle, ESD protection devices can be built inside and throughout an interposer, with proper layout planning and alignment so that the ESD switch devices can be connected to pads of chiplets to form a required ESD protection network. One key advantage for interposer-based ESD protection is that the core chip may be "free" of ESD protection devices, or may at least significantly reduce the ESD protection level for a core die (i.e., smaller and fewer ESD devices on a chip), which has been a large ESD design problem in advanced technologies [32,33]. Because of the lack of or reduced ESD protection burden on a chip die, the design of complex ICs in advanced technologies (e.g., very expensive 3 nm CMOS) will focus on delivering high performance, while saving the high-cost die area needed for on-chip ESD protection. Interposer ESD protection will play a more important role in SoICs because the high complexity of 3D heterogeneous chips makes ESD protection a much larger issue in μ-packaging, one for which interposer-based 3D ESD protection will be a vital reliability solution. For large, complex, high-performance chips, the benefits of using interposer-based ESD protection will be more significant because such chips have large numbers of pads (Figure 4); hence, removing/reducing ESD protection in core chips can substantially enhance chip performance while reducing chip costs.

More importantly, interposer-based ESD protection is naturally suitable for making a distributed ESD protection network, which is important for charged device model (CDM) ESD protection [34]. Compared with classic human body model ESD protection, CDM ESD is an emerging challenge for modern ICs in advanced technologies [35,36]. With reference to Figure 3, a human body model ESD is a "from-external-to-internal" event, one where the electrostatic charges of a pad originate externally; hence, traditional ESD protection relies on ESD protection structures at the pads (i.e., pad-based ESD protection) to discharge the incident static charges, i.e., preventing external charges from entering into a chip and, therefore, providing ESD protection [14]. On the other hand, CDM ESD is a "from-internal-to-external" phenomenon where static charges induced into a chip over the course of its lifetime are stored and distributed randomly inside an IC die [37]. Due to this unique nature of internal charge distribution, the classic pad-based CDM ESD protection

method, in usage for decades, is found to be fundamentally questionable, because when one pad is grounded during CDM ESD stressing, the internal charges must find ways to reach to the GND pad for discharging. Consequently, although at-pad ESD switch devices may conduct properly, the internal routing of ESD currents may still cause internal ESD failures, which is believed to be the main reason for the CDM ESD failure uncertainty that has recently emerged as a significant ESD reliability problem [34]. Clearly, the CDM ESD problem will be much more a design-for-reliability issue for SoICs in μ-packaging. The reason for this is that an SoIC chip has complex internal structures due to the many heterogeneous chiplets and to the packaging structure, making the internal storage of charges within SoICs/packaging much more significant and complicated. As a result, CDM ESD failure will be more uncertain and random, and CDM ESD protection becomes very difficult for SoICs in μ-packaging, something which in turn calls for ESD design innovation. Recently, a novel non-pad-based internally distributed CDM ESD protection method was reported to address this CDM ESD design problem [38]. Instead of using a pad-based CDM ESD protection method, the internally distributed CDM ESD protection method moves ESD switch devices from pads to the internal circuit nodes where static charges are likely stored, as illustrated in Figure 6. Therefore, when internal/local charges accumulate to a given level, the internal CDM ESD switch device will be turned on to discharge the charges locally/internally, without having to route through any complicated internal paths to reach to a GND pad for discharging. Hence, CDM ESD protection can be achieved. Clearly, interposer-based ESD protection offers the unique solution of internally distributed CDM ESD protection for SoICs in μ-packaging, one where local static charges can be readily discharged through ESD switch devices embedded in an interposer, and thus achieving robust CDM ESD protection for SoIC chips. Practically, various ESD switch devices may be used to build an interposer-based ESD protection network, for example, and as shown in Figure 7, an interposer might use vertical in-TSV ESD diodes [39].

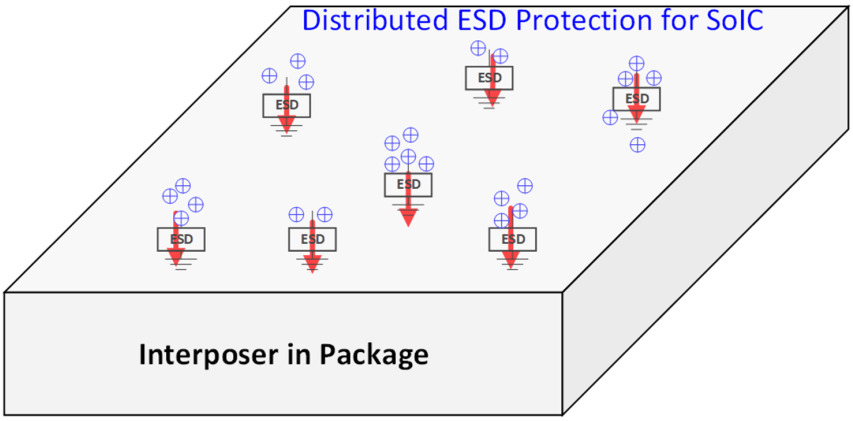

Figure 6. Concept of interposer-based internally distributed CDM ESD protection method.

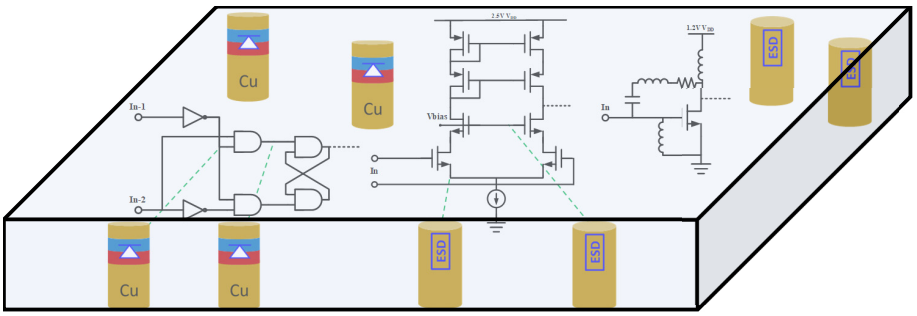

Figure 7. Illustration of internally distributed CDM ESD protection using vertical in-TSV ESD protection devices implemented in either a substrate or an interposer.

3. Proof of Concept Design Examples

Proof-of-concept prototype designs have been recently reported for interposer ESD protection for single chip [34,37]. A three-stage oscillator IC, designed and fabricated in a foundry with 45 nm SOI CMOS technology, was used as a test circuit. Figure 8 depicts the schematic for the oscillator chip that features classic pad-based CDM ESD protection using diode ESD devices at the pads. ESD simulation shows that, assuming that the ESD pulse comes to the pad externally and under 50 V CDM ESD stressing between V_{DD} pad and V_{SS} pad in both directions, ESD discharging occurs through the ESD diodes at the pads, as designed. Figure 9 presents the transient voltage behaviors of internal transistor voltage, e.g., V_{GS} and V_{GD} of MOSFET PM2, which is much lower than MOSFET breakdown voltage; hence CDM ESD protection seems to work. In accessing ESD protection, gate breakdown voltage is used as one ESD failure criterion, where BV_{OX} ~6.5 V for the 45 nm SOI technology used. Clearly, the traditional "from-external-to-internal" ESD zapping method does not truly reflect the CDM ESD discharging phenomenon, which is a "from-internal-to-external" event. Figure 10 depicts a real CDM ESD zapping scenario following the "from-internal-to-external" approach for the same IC, still featuring pad-based CDM ESD protection. Given that internal charge allocation/storage can be random, the CDM ESD stressing simulation considers three likely charge storage cases—splits 1, 2, and 3 as depicted in Figure 10. Figure 11 shows transient voltage behaviors for the selected internal MOSFET PM2 under the same 50 V CDM ESD zapping (note, discharging originates from internal nodes with one pad grounding). It is readily observed that PM2 fails under the internally oriented 50 V CDM ESD zapping, unlike that shown in Figure 9, hence confirming that classic pad-based CDM ESD protection may not work as expected. Figure 12 depicts the use of non-pad-based internally distributed CDM ESD protection for the same oscillator IC, whose transient voltage behaviors under same 50 V CDM zapping (internal-to-external zapping with one pad grounding) are also given in Figure 11. It is clearly seen that no voltage breakdown occurs, hence the IC successfully passed 50 V CDM ESD zapping. The interposer-based ESD protection concept was also validated experimentally using a single-pole four-throw (SP4T) RF switch circuit and a separate ESD interposer, which can be flip-chip bonded, as depicted in Figure 13 [37]. Figure 14 shows the fabricated SP4T core die (ESD-free) and interposer ESD die fabricated in a foundry 45 nm SOI CMOS technology. It is expected that the same interposer-based ESD protection method should work for SoICs in μ-packaging.

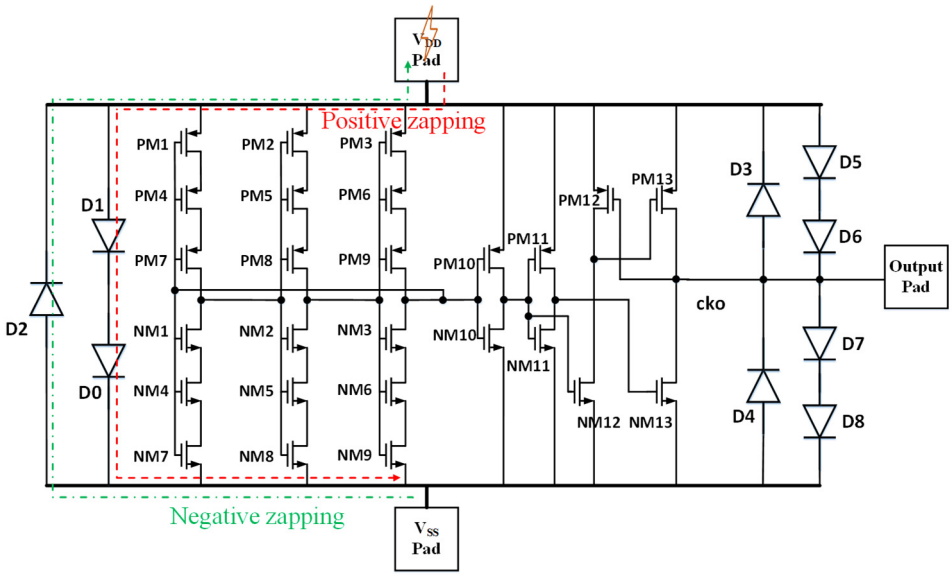

Figure 8. Schematic for a 3-stage oscillator IC featuring a classic pad-based CDM ESD protection network. Under typical CDM ESD zapping (traditional external-to-internal stressing at pad) between

V_{DD} pad and V_{SS} pad in both directions, ESD discharging occurs through ESD diodes as designed (dashed-lines indicating ESD discharging paths) [34].

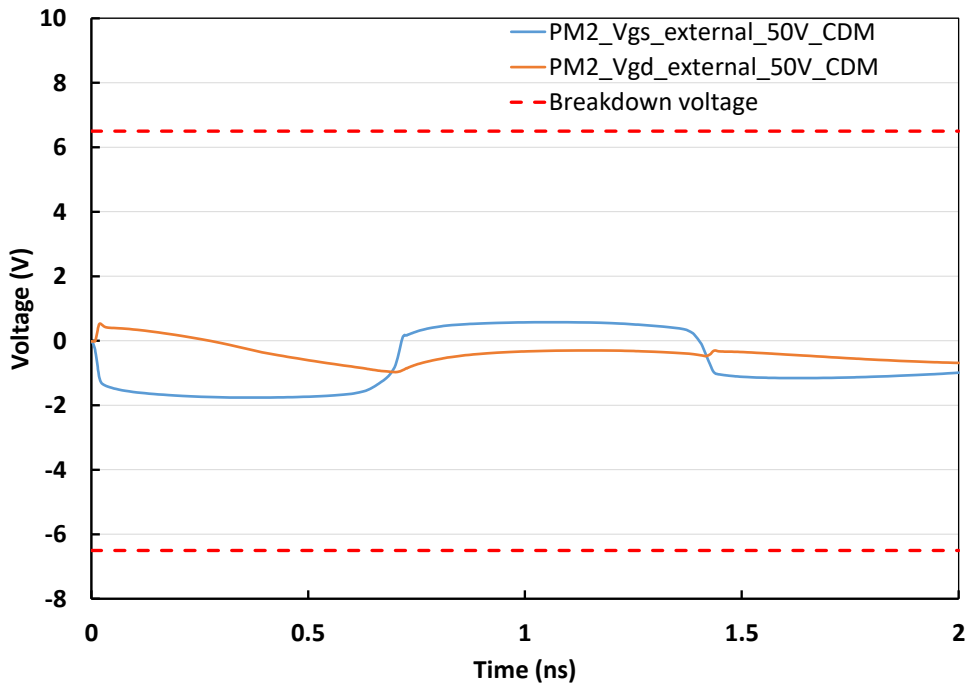

Figure 9. Transient voltage behaviors (V_{GS}, V_{GD}) of PM2 of the IC in Figure 8 under 50 V CDM ESD stressing (traditional external zapping to pad), suggesting classic pad-based CDM ESD protection seems to be "working" [34].

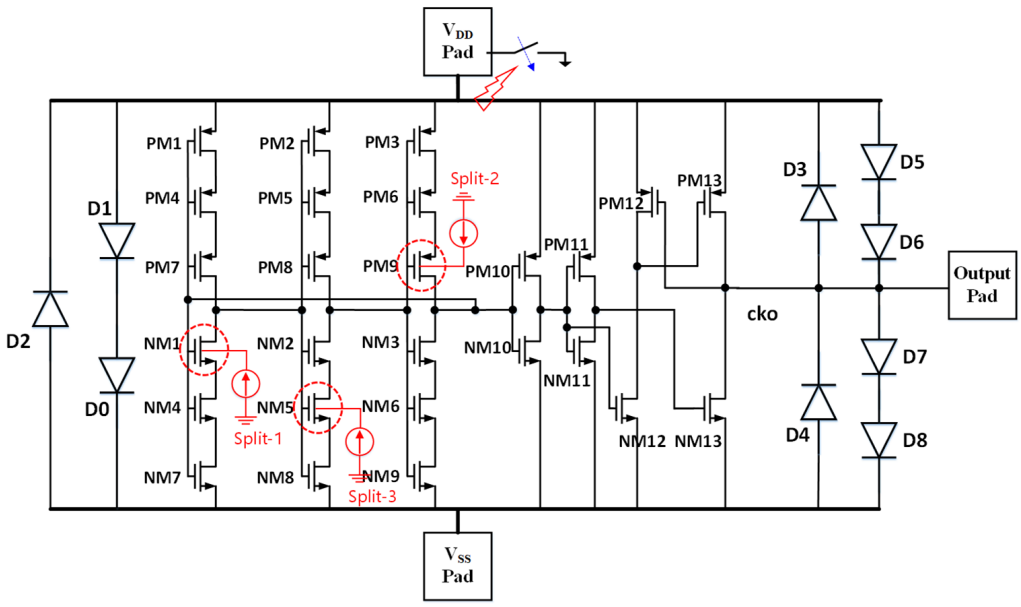

Figure 10. Using the internally oriented CDM ESD zapping (internal-to-external discharging with a pad grounding) method for the same oscillator IC, still using classic pad-based CDM ESD protection. Splits 1, 2 and 3 show three different internal charge storage cases [37].

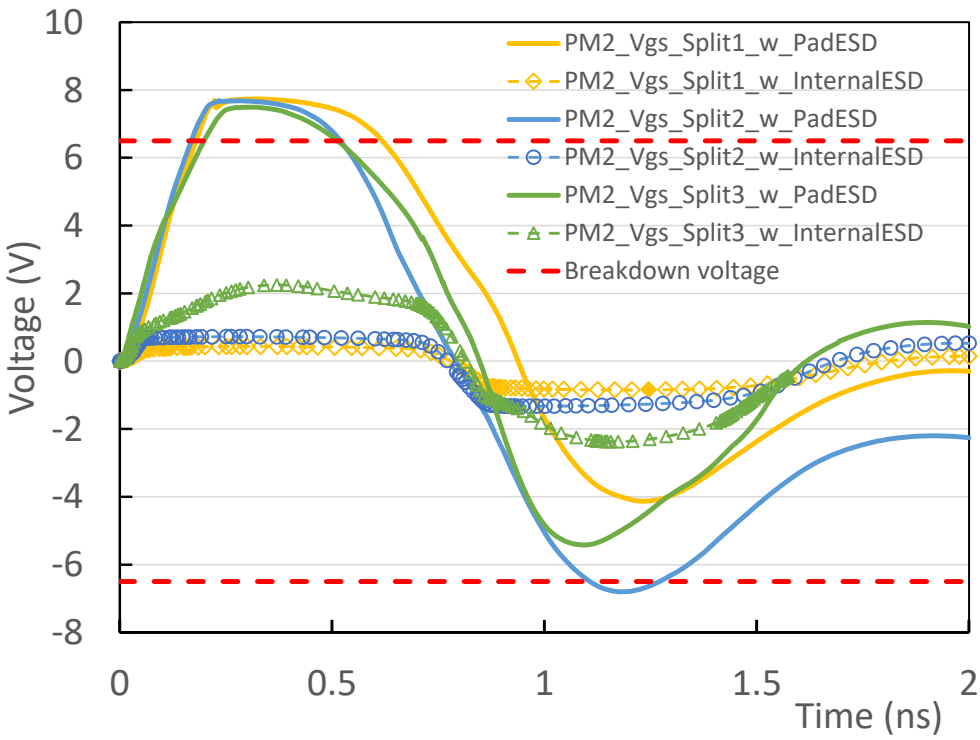

Figure 11. Transient voltage behaviors for typical internal PM2 under internally oriented CDM ESD zapping show that 50 V CDM ESD stressing causes breakdown ESD failure if using classic pad-based CDM ESD protection (solid lines); however, using internally distributed CDM ESD protection (hollow marks) passes 50 V CDM ESD zapping [37].

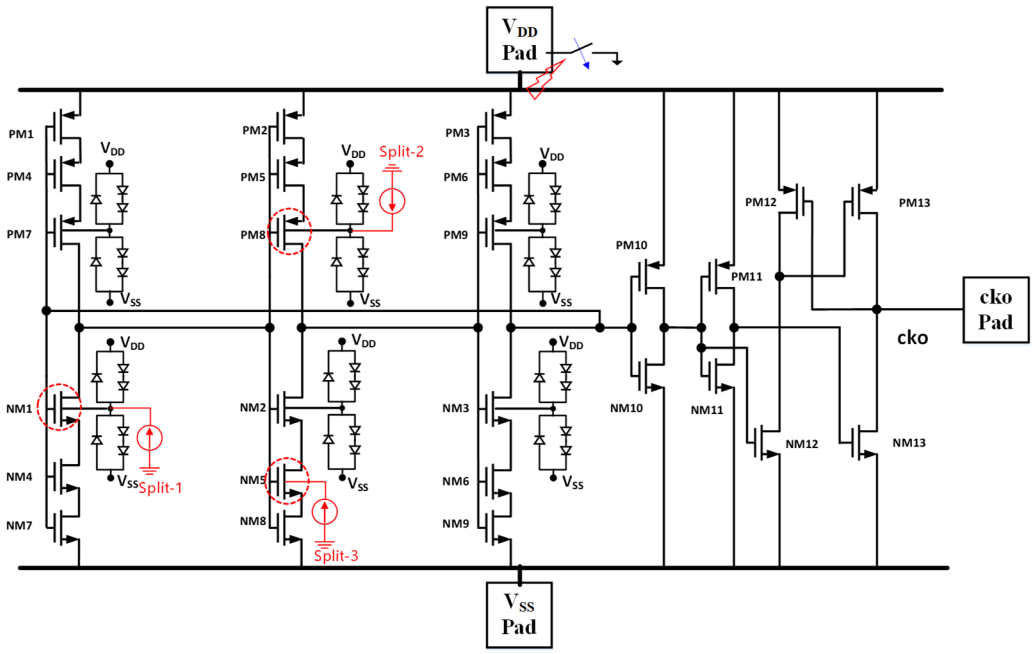

Figure 12. Same oscillator IC uses non-pad internally distributed CDM ESD protection. Applying internally oriented CDM ESD zapping (internal-to-external discharging with one pad grounding). Splits 1, 2, and 3 show three different internal charge storage cases [37].

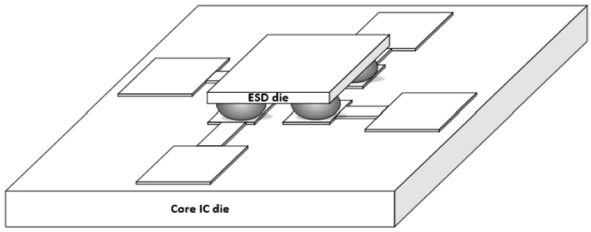

Figure 13. Conceptual illustration of interposer-based ESD protection flip-chip bonded with an ESD-free core die [37].

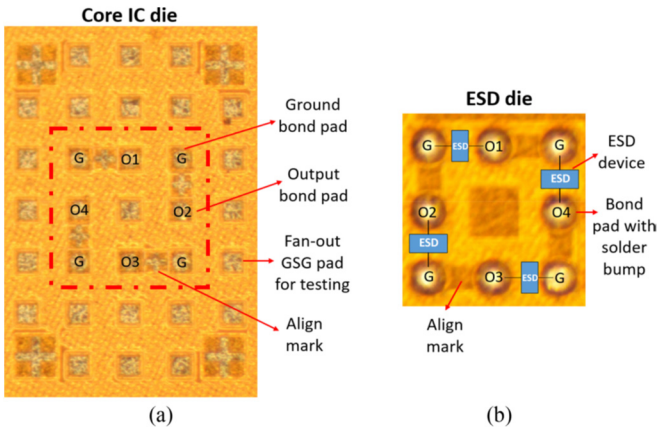

Figure 14. Die photos for an ESD-free SP4T circuit core die (**a**) and a separate interposer ESD die (**b**) [37].

4. Interposer-Based ESD Protection Design Challenges

Though very promising, the realization of interposer-based ESD protection for SoICs in μ-packaging will face two major design challenges. First, a new holistic cross-layer/domain ESD protection approach is highly desired for interposer-based ESD protection designs due to the fact that SoICs in μ-packaging involve many, and continuously increasing, chiplets/dielets, different materials and intermediate layers in packaging. Furthermore, many different process technologies are typically used to fabricate different chiplets by different chip vendors. Hence, complying with the ESD design windows (Figure 2b) for all chiplets within one packaging is certainly very difficult. More importantly, holistic ESD protection in packaging will be required to minimize overall ESD design overhead effects that will seriously affect the performance, reliability and costs of SoIC superchips. This is because smart partitioning and allocation of ESD protection switch devices among individual chiplets and packaging media may help to reduce the head counts of all in-packaging ESD protection devices, while still maintaining robust SoIC ESD protection. Relying on local ESD protection on individual chiplets and counting on the simple "stacking" result of SoICs in μ-packaging will not be acceptable. Second, it is well known that a CAD-based design methodology is essential to ESD protection designs for monolithic SoC IC chips in order to achieve ESD protection design optimization, validation and prediction [19]. The same principle applies to holistic ESD protection designs for SoICs in μ-packaging. Due to increased domain/structural complexity, the design and implementation of interposer-based ESD protection for SoICs in μ-packaging will be extremely challenging, such that it could only be tackled by CAD-based design methodologies. Some specific ESD design difficulties include holistic ESD protection co-simulation (atom to system) among all elements in a package; addressing complex interfacing effects across different chiplets and packaging layers and materials; modeling complex boundary conditions and interactions of packaging (e.g., thermal, mechanical effects); including packaging in ESD simulation; new modeling and CAD algorithms and tools to support the above tasks; and new testing

techniques to validate ESD protection designs in packaging. All of these are non-trivial R&D tasks for the future. It is also noteworthy that artificial intelligence (AI) techniques will play an important role in developing ESD protection solutions for SoICs in μ-packaging. Particularly, ESD-specific (i.e., scientific) AI models and algorithms should be explored for holistic ESD protection, e.g., modeling internal charge allocation, smart partitioning of SoICs and allocation of ESD protection elements within μ-packaging, to minimize total ESD design overhead effects while achieving high performance and the robust ESD protection of SoICs [17]. We believe that this will be a new ESD protection design area that will attract increasing R&D efforts in the future.

5. Summary

Performance and reliability are two core attributes for ICs, including SoICs in advanced packaging. ESD failure is a major IC reliability problem and ESD protection is an emerging design challenge for SoICs in μ-packaging. This article discusses key perspectives for ESD protection research for hetero-integrated SoIC chips, for which interposer-based ESD protection is considered an important potential solution for smart future chips in advanced packaging, one which is articulated using design prototypes. Key design challenges and research directions for exploring holistic ESD protection for SoICs in μ-packaging are highlighted.

6. Patents

A. Wang: "Interposer-based ESD Protection Structures", *U.S. Patent* filed, #62/412,105, 2016.

Author Contributions: All co-authors (X.L., Z.P., W.H., R.M. and Z.Y.) contributed to writing and data analysis. Conceptualization by A.W. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data are contained within the article.

Acknowledgments: We acknowledge support from GlobalFoundries for fabricating design examples.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

CDM	Charged device model
CMOS	Complementary metal-oxide-semiconductor
ESD	Electrostatic discharge
HBM	Human body model
HI	Heterogeneous integration
IC	Integrated circuit
SoC	System-on-a-chip
SOI	Silicon-on-insulator
SoIC	Systems-on-integrated-chiplets

References

1. Brattain, W.H. *Entry of 15 December 1947, Laboratory Notebook, Case 38139-7*; Bell Laboratories Archives: Murray Hill, NJ, USA, 1947.
2. Shockley, W. Circuit Element Utilizing Semiconductor Material. U.S. Patent 2,569,347A, 25 September 1951.
3. Shockley, W. Semiconductor Amplifier. U.S. Patent 2,502,488A, 4 April 1950.
4. Kilby, J.S. Miniaturized Electronic Circuits. U.S. Patent 3,138,743, 23 June 1964.
5. Moore, G.E. Cramming more components onto integrated circuits. *Electronics* **1965**, *38*, 114–117. [CrossRef]

6. IEEE Electronics Packaging Society. *HIR: Heterogeneous Integration Roadmap, Edition 2024*; IEEE Electronics Packaging Society: Piscataway, NJ, USA, 2024. Available online: https://eps.ieee.org/technology/heterogeneous-integration-roadmap/hir-special-sessions-at-estc-2024.html (accessed on 23 March 2025).
7. Li, X.; Pan, Z.; Hao, W.; Miao, R.; Yue, Z.; Wang, A. Enhancing Chip Performance and Reliability by CMOS+X Technologies. *Appl. Phys. Rev.* **2024**, *11*, 021331. [CrossRef]
8. CoWoS. TSMC. Available online: https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/cowos.htm (accessed on 23 March 2025).
9. Banijamali, B.; Chiu, C.-C.; Hsieh, C.-C.; Lin, T.-S.; Hu, C.; Hou, S.-Y.; Ramalingam, S.; Jeng, S.-P.; Madden, L.; Yu, D.C.H. Reliability evaluation of a CoWoS-enabled 3D IC package. In Proceedings of the IEEE 63rd Electronic Components and Technology Conference, Las Vegas, NV, USA, 28–31 May 2013; pp. 35–40.
10. Pan, Z.; Li, X.; Hao, W.; Miao, R.; Wang, A. Design for EMI/ESD Immunity for Flexible and Wearable Electronics. *IEEE J. Electron Devices Soc. (J-EDS)* **2023**, *11*, 700–707. [CrossRef]
11. Liang, S.W.; Liang, Y.R.; Wu, G.C.Y.; Yee, K.C.; Wang, C.T.; Yu, D.C.H. Reliability Performance on Fine-Pitch SoI Bond. In Proceedings of the IEEE Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 30 May–2 June 2023; pp. 783–787.
12. Lu, R.; Chuang, Y.-C.; Wu, J.-L.; He, J. Reliability Challenges from 2.5D to 3DIC in Advanced Package Development. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 26–30 March 2023.
13. Pan, Z.; Li, C.; Hao, W.; Li, X.; Wang, A. ESD Protection Designs: Topical Overview and Perspective. *IEEE Trans. Device Mater. Reliab. (TDMR)* **2022**, *22*, 356–370. [CrossRef]
14. Wang, A. *Practical ESD Protection Design*; Wiley-IEEE Press: New York, NY, USA, 2022; ISBN 978-1119850403.
15. Voldman, S. *ESD: RF Technology and Circuits*; Wiley: Hoboken, NJ, USA, 2006; ISBN-13: 978-0470847558.
16. Semiconductor Market Size Worldwide by Application, ASML Via STATISTA, Yahoo!Finance. Available online: https://www.yahoo.com/finance/news/biden-has-big-plans-for-semiconductor-clusters--will-companies-play-along-200042981.html (accessed on 3 March 2023).
17. Hao, W.; Pan, Z.; Li, X.; Miao, R.; Yue, Z.; Wang, A. On-Chip ESD Protection: Design Innovation. *IEEE Electron Devices Rev.* **2024**, *2*, 32–51. [CrossRef]
18. Li, X.; Pan, Z.; Hao, W.; Miao, R.; Yue, Z.; Wang, A. On-Chip ESD Protection: Device Innovation. *IEEE Electron Devices Rev.* **2024**, *1*, 1–15. [CrossRef]
19. Pan, Z.; Li, X.; Hao, W.; Miao, R.; Wang, A. On-Chip ESD Protection Design Methodologies by CAD Simulation. *ACM Trans. Des. Autom. Electron. Syst. (TODAES)* **2023**, *29*, 1–41. [CrossRef]
20. Di, M.; Pan, Z.; Zhang, F.; Li, C.; Wang, H.; Wang, A. A Study of ESD-mmWave-Switch Co-Design of 28GHz Distributed Travelling Wave Switch in 22nm FDSOI for 5G Systems. *IEEE J. Electron Devices Soc. (J-EDS)* **2021**, *6*, 1290–1296. [CrossRef]
21. IEEE Electronics Packaging Society. Chapter 22: Interconnects for 2D and 3D Architectures. In *HIR: Heterogeneous Integration Roadmap, Edition 2024*; IEEE Electronics Packaging Society: Piscataway, NJ, USA, 2024.
22. Knickerbocker, J.U.; Andry, P.S.; Dang, B.; Horton, R.R.; Patel, C.S.; Polastre, R.J.; Sakuma, K.; Sprogis, E.S.; Tsang, C.K.; Webb, B.C.; et al. 3D silicon integration. In Proceedings of the Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, USA, 27–30 May 2008; pp. 538–543.
23. Ogutu, P.; Fey, E.; Dimitrov, N. Superconformal filling of high aspect ratio through glass vias (TGV) for interposer applications using TNBT and NTBC additives. *J. Electrochem. Soc.* **2015**, *162*, D457. [CrossRef]
24. Hamelink, J.; Poelma, R.H.; Kengen, M. Through-polymer-via for 3D heterogeneous integration and packaging. In Proceedings of the IEEE 17th Electronics Packaging and Technology Conference (EPTC), Singapore, 2–4 December 2015; pp. 1–7.
25. Martwick, A.; Drew, J. Silicon Interposer and TSV Signaling. In Proceedings of the IEEE 65th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 26–29 May 2015; pp. 266–275.
26. Zaghari, P.; Sinha, S.S.; Hopkins, D.C.; Ryu, J.E. Co-Design and ML-Based Optimization of Through-Via in Silicon and Glass Interposers for Electronic Packaging Applications. *IEEE Trans. Compon. Manuf. Technol.* **2025**, *15*, 295–308. [CrossRef]
27. Cai, M.; Ling, B.; Chen, D.; Xia, Y.; Wang, H.; Han, Y.; Wu, Y. Double-layer-stacked Silicon Interposer for 2.5D Packaging of 32×32 Micromirror Array Chip. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2025**, *15*, 706–715. [CrossRef]
28. Kim, J. Active Si Interposer for 3D IC Integrations. In Proceedings of the 2015 International 3D Systems Integration Conference (3DIC), Sendai, Japan, 31 August–2 September 2025.
29. Liu, Y.; Li, D.; Yang, Z.; Zhang, C.; Zhang, Y.; Li, X.; Cao, M.; Yin, S. A Chiplet Platform for Intelligent Radar/Sonar Leveraging Domain-Specific Reusable Active Interposer. *IEEE. Trans. Very Large Scale Integr.* **2025**, *33*, 903–915. [CrossRef]
30. Jiao, B.; Zhu, H.; Zeng, Y.; Li, Y.; Liao, J.; Jia, S.; Chen, Z.; Tian, M.; Zhu, J.; Wen, D.; et al. 37.4 SHINAI: A 586 mm^2 Reusable Active TSV Interposer with Programmable Interconnect Fabric and 512 Mb 3D Underdeck Memory. In Proceedings of the 2025 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 16–20 February 2025.

31. Jayabalan, J.; Chidambaram, V.; Siang, S.L.P.; Wang, X.; Chinq, J.M.; Bhattacharya, S. Active Through-Silicon Interposer Based 2.5D IC Design, Fabrication, Assembly and Test. In Proceedings of the IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 28–31 May 2019; pp. 587–593.
32. Industry Council on ESD Target Levels. *White Paper 1: A Case for Lowering Component Level HBM ESD Specifications and Requirements, Industry Council on ESD Target Levels, Rev. 4.0*; Industry Council on ESD Target Levels: Online, 2018.
33. Industry Council on ESD Target Levels. *White Paper 2: A Case for Lowering Component-Level CDM ESD Specifications and Requirements, Industry Council on ESD Target Levels, Rev. 3.0*; Industry Council on ESD Target Levels: Online, 2021.
34. Di, M.; Li, C.; Pan, Z.; Wang, A. Pad-Based CDM ESD Protection Methods Are Faulty. *IEEE J. Electron Devices Soc. (J-EDS)* **2020**, *8*, 1297–1304. [CrossRef]
35. *ANSI/ESDA/JEDEC JS-001-2017*; For Electrostatic Discharge Sensitivity Testing—Human Body Model (HBM)—Component Level. ESD Association: Rome, NY, USA; JEDEC: Arlington, VA, USA, 2017.
36. *ANSI/ESDA/JEDEC JS-002-2018*; For Electrostatic Discharge Sensitivity Testing—Charged Device Model (CDM)—Device Level. ESD Association: Rome, NY, USA; JEDEC: Arlington, VA, USA, 2018.
37. Di, M.; Li, C.; Pan, Z.; Wang, A. Non-Pad-Based in Situ in-Operando CDM ESD Protection Using Internally Distributed Network. *IEEE J. Electron Devices Soc. (J-EDS)* **2021**, *9*, 1248–1256. [CrossRef]
38. Wang, A. Interposer-Based ESD Protection Structures. U.S. Patent 62/412,105, 25 October 2016.
39. Li, C.; Di, M.; Pan, Z.; Wu, H.; Wang, A. Vertical TSV-Like Diode ESD Protection. In Proceedings of the IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Chengdu, China, 9–12 March 2021; pp. 676–678.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.